What is claimed is:

1. A data transfer control system for data transfer through a bus, comprising:

a command processing section which receives a command packet transferred through a first bus, issues a command indicated by the command packet to a device connected to a second bus, and orders start of a direct memory access (DMA) transfer through the second bus; and

a command abort section which aborts the command issued to the device connected to the second bus based on the command packet after the completion of the DMA transfer started based on the command packet.

2. The data transfer control system as defined in claim 1, further comprising:

a command comparison section which compares contents of a first command packet transferred through the first bus before a bus reset with contents of a second command packet transferred through the first bus after the bus reset, when the bus reset that clears node topology information has occurred during the processing of the first command packet,

wherein the command abort section aborts a command which has been issued to the device connected to the second bus based on the first command packet after completion of a DMA transfer which has been started based on the first command packet, when the contents of the first command packet are determined to be different from the contents of the second command packet.

3. The data transfer control system as defined in claim 1, wherein:

when a bus reset that clears node topology information occurs during processing of a first command packet,

in a case where a command of the first command packet has been issued to the

device connected to the second bus, the command of the first command packet is aborted, and

in a case where the command of the first command packet has not been issued to the device connected to the second bus, processing of a second command packet starts without aborting the command of the first command packet.

4. The data transfer control system as defined in claim 1,

wherein the command abort section controls dummy data transfer to or from the device connected to the second bus until the completion of the DMA transfer.

5. The data transfer control system as defined in claim 4,

wherein the command abort section aborts a command without controlling dummy data transfer when any DMA transfer is not being performed in determination of whether or not the command is to be aborted.

6. The data transfer control system as defined in claim 4, further comprising:

a pointer management section which manages pointers for a packet buffer which is a ring buffer and temporarily stores transferred data, the pointer management section updating a first pointer each time when data transferred from the second bus is written in the packet buffer, and also updating a second pointer each time when data to be transferred to the first bus is read from the packet buffer,

wherein the command abort section controls dummy data transfer by performing a dummy update on the second pointer so that the first pointer does not go ahead of the second pointer.

7. The data transfer control system as defined in claim 4, further comprising:

a pointer management section which manages pointers for a packet buffer

which is a ring buffer and temporarily stores transferred data, the pointer management section updating a third pointer each time when data to be transferred to the second bus is read from the packet buffer, and also updating a fourth pointer each time when data transferred from the first bus is written in the packet buffer,

wherein the command abort section controls dummy data transfer by performing a dummy update on the fourth pointer so that the third pointer does not go ahead of the fourth pointer.

8. The data transfer control system as defined in claim 1,

wherein the first bus transfers data conforming to the IEEE 1394 standard, and the second bus transfers data conforming to the Advanced Technology Attachment/Advanced Technology Attachment Packet Interface (ATA/ATAPI) standard.

9. An electronic instrument comprising:

the data transfer control system as defined in claim 1; and

the device connected to the second bus.

10. A program causing a data transfer control system to function as:

a command processing section which receives a command packet transferred through a first bus, issues a command indicated by the command packet to a device connected to a second bus, and orders the start of a direct memory access (DMA) transfer through the second bus; and

a command abort section which aborts the command issued to the device connected to the second bus based on the command packet after the completion of the DMA transfer started based on the command packet.

11. The program as defined in claim 10 causing the data transfer control system to

further function as:

a command comparison section which compares contents of a first command packet transferred through the first bus before a bus reset with contents of a second command packet transferred through the first bus after the bus reset, when the bus reset that clears node topology information has occurred during the processing of the first command packet,

wherein the command abort section aborts a command which has been issued to the device connected to the second bus based on the first command packet after completion of a DMA transfer which has been started based on the first command packet, when the contents of the first command packet are determined to be different from the contents of the second command packet.

12. The program as defined in claim 10,

wherein the command abort section controls dummy data transfer to or from the data transfer control system and the device connected to the second bus until the completion of the DMA transfer.

13. A data transfer control method for data transfer through a bus, the method comprising:

issuing a command indicated by a command packet transferred through a first bus, to a device connected to a second bus, and ordering start of a direct memory access (DMA) transfer through the second bus; and

aborting the command issued to the device connected to the second bus based on the command packet after the completion of the DMA transfer started based on the command packet.

14. The data transfer control method as defined in claim 13, further comprising:

comparing contents of a first command packet transferred through the first bus before a bus reset with contents of a second command packet transferred through the first bus after the bus reset, when the bus reset that clears node topology information has occurred during the processing of the first command packet; and

aborting a command which has been issued to the device connected to the second bus based on the first command packet after completion of a DMA transfer which has been started based on the first command packet, when the contents of the first command packet are determined to be different from the contents of the second command packet.

15. The data transfer control method as defined in claim 13, when a bus reset that clears node topology information occurs during processing of a first command packet, further comprising:

aborting a command of the first command packet, in a case where the command of the first command packet has been issued to the device connected to the second bus; and

starting processing of a second command packet without aborting the command of the first command packet, in a case where the command of the first command packet has not been issued to the device connected to the second bus,.

16. The data transfer control method as defined in claim 13, further comprising:

controlling dummy data transfer to or from the device connected to the second bus until the completion of the DMA transfer.

17. The data transfer control method as defined in claim 16, further comprising:

aborting a command without controlling dummy data transfer when any DMA transfer is not being performed in determination of whether or not the command is to be

aborted.

18. The data transfer control method as defined in claim 16, further comprising:

managing pointers for a packet buffer which is a ring buffer and temporarily stores transferred data, a first pointer being updated each time when data transferred from the second bus is written in the packet buffer, and a second pointer being updated each time when data to be transferred to the first bus is read from the packet buffer; and

controlling dummy data transfer by performing a dummy update on the second pointer so that the first pointer does not go ahead of the second pointer.

19. The data transfer control method as defined in claim 16, further comprising:

managing pointers for a packet buffer which is a ring buffer and temporarily stores transferred data, a third pointer being updated each time when data to be transferred to the second bus is read from the packet buffer, and a fourth pointer being updated each time when data transferred from the first bus is written in the packet buffer; and

controlling dummy data transfer by performing a dummy update on the fourth pointer so that the third pointer does not go ahead of the fourth pointer.

20. The data transfer control method as defined in claim 13,

wherein the first bus transfers data conforming to the IEEE 1394 standard and the second bus transfers data conforming to the Advanced Technology Attachment/Advanced Technology Attachment Packet Interface (ATA/ATAPI) standard.